TOWARDS A PROCESS VARIATION AWARE DELAY MODEL FOR FPGA YIELD ENHANCEMENT

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ABSTRACT

In this paper, a study towards building a complete analytical delay model of an FPGA considering process variation is presented. The model could allow designers to gain insight into how transistor-level design parameters (e.g. transistor size, V_{dd} and V_{th}) affects nominal delay and delay distribution. We extract the entire FPGA circuits into very simple primitives , inverter and pass transistor. A script translates block level critical path generated by VPR [1] into transistor level netlists which could be used for both HSPICE and our analytical model. An investigation of yield enhancement by varying transistor size, V_{dd} and V_{th} could be achieved.

1. INTRODUCTION

As semiconductor feature sizes continue to scale down, process variation becomes a critical issue. Most of the literature concerning the design of FPGAs has employed optimisation of delay models in order to minimise delay [1]. This approach has two shortcomings, firstly that this gives little information about the effect of different parameters on the delay function, and secondly effects of process variations are not considered. This work presents a closed-form analytic delay model which includes statistical variation.

In an integrated circuit, sources of variability include imperfections in: [2]

- photolithography and etching leading to deviation of device width and length
- the deposition and growth process, as well as chemical-mechanical planarization, film thickness cannot be controlled in a uniform manner
- properties of transistors being affected by the temperature of the annealing process.

In this work we limit our study to variation in threshold voltage (V_{th}) which has one of the largest contributions to statistical delay distribution.

Unlike ASIC, critical path of FPGA could not be predicted before the real circuits are implemented. However, for both deterministic delay optimisation and yield enhancement, the critical path is needed. Therefore, to use multiple most representative benchmark circuits to evaluate yield performance of FPGA becomes a common way. The author employ the same strategy in the proposed research.

The rest of this paper is organized as following. Section 2 introduces primitive circuits for modelling FPGAs. A detailed delay model is introduced in section 3 and variation of V_{th} is presented in section 4. A complete workflow of yield enhancement is described in section 5 Finally, conclusions and future work are discussed in section 6.

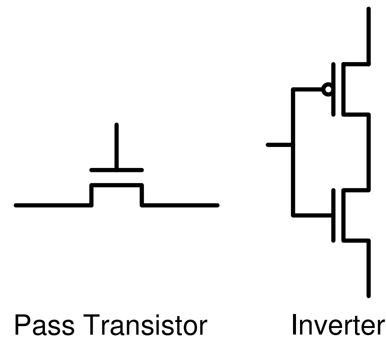

Fig. 1. Primitives of FPGA

2. DELAY PRIMITIVES

An island-style FPGA is normally composed of logic blocks, connection blocks and switch boxes [1]. These can be built from the primitives illustrated in figure 1.

The pass transistor is used to build multiplexers for look-up tables (LUT), connection boxes and tristate buffers. The inverter can be used as buffers or sense buffers. Sense buffers always follow pass transistors to restore the threshold voltage drop introduced when a high input is present. The sense buffer is an inverter, with the P/N ratio adjusted to move its switching point to compensate for the pass transistor threshold voltage drop.

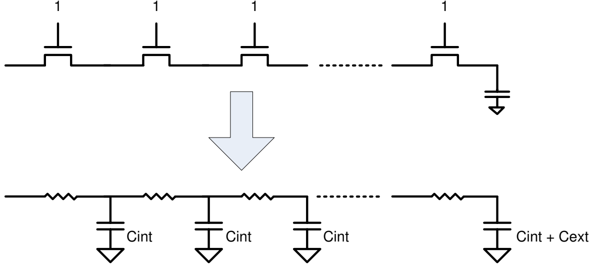

Fig. 2. RC model of cascading multiple stage pass transistors

At the transistor level, PMOS transistors are used as pull-up devices in inverters, serving to charge load capacitances. NMOS transistors are used in two different ways: pass transistors and pull-down circuits in inverters. The equivalent resistance of a pass transistor and inverter are different due to the body effect in the former.

3. MODEL

In our model, all the primitive circuits are modelled as an equivalent RC network. The formula for deriving equivalent resistance is [3]

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \quad (1)$$

$$I_{DSAT} = \beta(V_{DSAT}V_{DD} - \frac{V_{DSAT}^2}{2}) \quad (2)$$

$$\beta = k'\frac{W}{L} \quad (3)$$

For an inverter, with load capacitance C_l,

$$Delay = 0.69 R_{eq} C_l \quad (4)$$

For multiple cascaded pass transistors in figure 2, Elmore delay model could be applied,

$$\begin{aligned} Delay &= R_{eq}C_{int} + 2R_{eq}C_{int} + \dots \\ &\quad +(n-1)R_{eq}C_{int} + nR_{eq}C_l \\ &= \frac{n(n-1)}{2}R_{eq}C_{int} + nR_{eq}C_l \end{aligned} \quad (5)$$

4. VARIATION OF V_{TH}

To understand the delay distribution, it is necessary to model how V_{th} changes with transistor size.

For short channel transistors, variability of threshold voltage is predominantly determined by the transistor's geometries, in particular effective channel length [4].

A well known relationship between threshold voltage variance and area of active region can be expressed as,

$$\sigma_{\Delta} = \frac{A_{\Delta V_t}}{\sqrt{WL}} \quad (6)$$

where $A_{\Delta V_t}$ is a technology conversion constant (in mVμm), and WL is transistor active region area. In TSMC 0.18μm technology, gate oxide thickness (t_{ox}) is $4nm$ and $A_{\Delta V_t}$ is 7.00 mVμm. Figure 3 shows how V_{th} changes with transistor width. Figure 4 presents V_{th} distributions for transistor widths of 2λ, 10λ and 20 λ respectively.

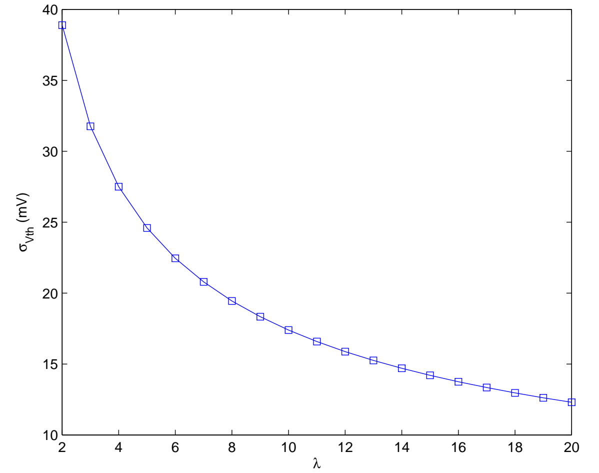

Fig. 3. Threshold Voltage Variation vs Size

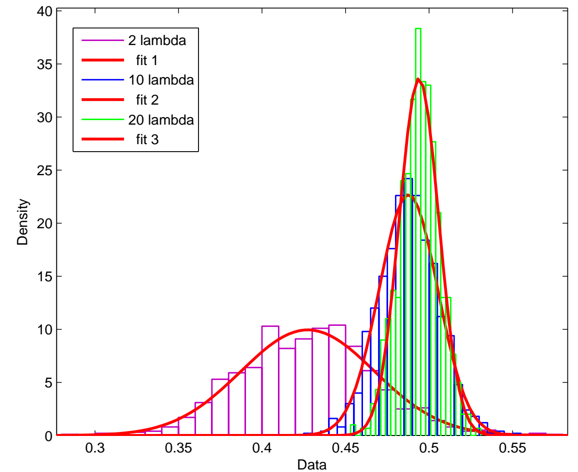

Fig. 4. Threshold Voltage Distribution of 2λ 10λ and 20 λ

5. WORKFLOW OF YIELD ENHANCEMENT

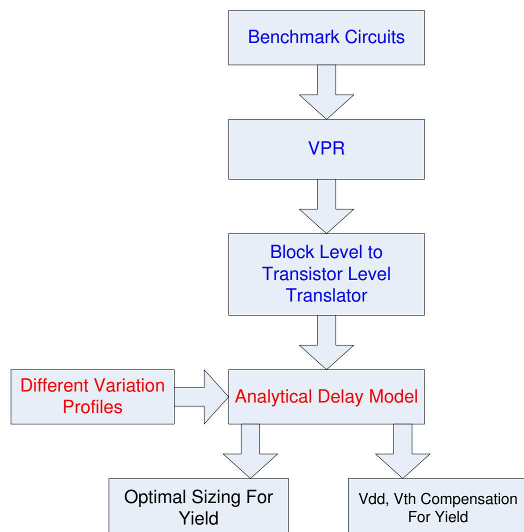

Fig. 5. Workflow of Yield Enhancement

Figure 5 presents the whole workflow of yield enhancement. Blocks with blue words represents existing work. The analytical delay model is in progress as described in section 3. For the part of process variation profiles, a technique using ring oscillator array to abstract process variation profiles from real FPGA was introduced in [5]. In [2], Pang et al made a thorough study on process variliabity in 90nm technology by building a real test chip. Based on these work, it is feasible to develop a reasonable within-die variation model.

Several works show that adjusting on transistor sizes, v_{dd} and V_{th} would reduce yield loss significantly. Yield enhancement using sizing scheme was introduced in [6]. In [7], Bijansky et al study an FPGA architecture with dual voltage supply wherein the supply voltage for individual CLBs can be assigned after fabrication. Post-manufacturing tuning can increase the yield up to 10× with conventional design. An process variation tolerant architecture with adaptive body bias compensation was described in [8], with such scheme, delay variation is reduced by 30% and the leakage variability is reduced by 78%. In our work, a universal delay model would be built to cover all the above works within a framework, which delivers much more insights for FPGA architect.

6. CONCLUSION AND FUTURE WORK

A delay model for PMOS and NMOS transistors based on RC analysis have been derived and can be used to model an FPGA. And a workflow targeting for yield enhancement based on such delay model is described.

In future work, we will explore the following issues.

- Model the effect of input slope on primitive delay. At the first stage, a delay model for primitives is derived for a step input. Experiment shows input slope greatly affects propagation delay. To investigate the real circuits path delay is not as simple as to sum up individual delay of primitives. They correlate with each other very much.
- Study how multiple process parameters can affect V_{th}, e.g. flat-band voltage, gate oxide thickness, substrate dopant, channel length through the short-channel effect and reverse-short-channel effect, and channel width through the narrow-width and inverse-narrow-width effect [9]. We can also include more fundamental physical parameters to improve accuracy and robustness and understand how process technology affects FPGA architectural level performance.
- Finally, after gaining more insight into how process parameters affect the performance of an FPGA, it may be possible to develop better process variation tolerant architectures.

7. REFERENCES

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