FPGA INTERCONNECT SIZING USING EXTENDED LOGICAL EFFORT MODEL

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1. INTRODUCTION

In a field programmable gate array (FPGA), the interconnect network typically dominates all key metrics: area, delay and power. Techniques to optimize interconnect at both architectural and circuit levels is an important problem in their design. This is typically done by studying architectural issues using tools such as VPR, and circuit issues and transistor sizing through Spice simulation (e.g. [1]). Unfortunately, such simulations do not offer much insight into dominant sources of delays and minimal achievable delay, nor do they help in sizing if multiple transistors are considered. To address this problem we have applied logical effort (LE) [2] to develop closed-form expressions for calculating delay, sensitivity to delay, optimal transistor sizing and a lower bound for delay [3]. In this work, we propose an improved model that relies on fewer primitive elements.

Moreover, as CMOS devices scale down to deep submicron and even nanometer levels, process variation affects yield and performance much more than ever before. Parametric variability is also considered in this work. Since parameters such as effective channel length, oxide thickness and threshold voltage, used in the extended logical effort (XLE) [4] model are related to process variation, we aim to establish analytical closed form relationships between delay and process variation. Using such a model, statistical analysis can be done on FPGA interconnect and techniques such as statistical sizing optimization [5] can be applied to improve yield with consideration of process variation. To the best of the author's knowledge, no previous work in applying XLE to interconnect modelling or process variation has been reported.

2. TARGET ARCHITECTURE AND PRIMITIVES

In the first instance, we study tristate driver interconnect in FPGA (figure 2) [1]. From the figure, we can see the components are sense buffer, multiplexer, active driver and pass-transistor. Essentially, only two primitives need to be modeled, pass-transistors and inverters, as the other circuit elements are compositions using them.

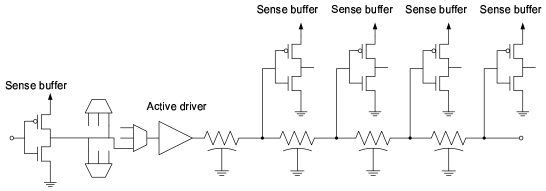

Fig. 1. Single-driver model

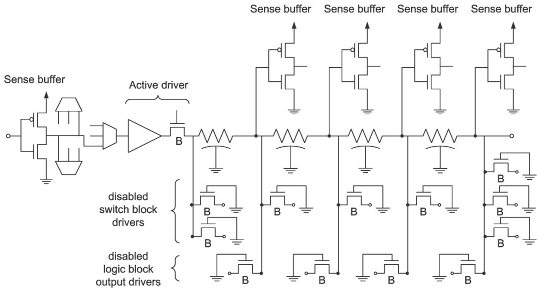

Fig. 2. Tristate-driver model

We previously used classical logical effort to model the inverter. The estimation of delay and its sensitivity to size is acceptable for interconnect circuits but the linear representation used, cannot accurately model non-linear features. As device sizes go down, non-linear effects become more significant. Therefore, we apply an extended logical effort (XLE) method to model CMOS combinatorial gate delay (simply an inverter for an interconnect model). In [4], Lasbouygues et al developed a more sophisticated model that takes into consideration I/O coupling and input ramp effects that distinguish the transition time from the propagation delay. In this work, we would apply this technique to interconnect circuit modelling. Thus new method assures a better approximation to simulation results than previous one, because classical LE model fails to be input-slope aware, which typically underestimates delays. We can change any single primitive and determine the performance change, making it a more flexible method to tune device sizes. Also, in the XLE model, effective channel length (L_{eff}), oxide thickness (t_{ox}) and threshold voltage

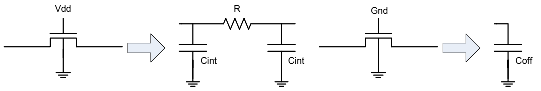

Fig. 3. Pass transistor modelling

(V_{th}) are modelled directly. When considering process variation, these become stochastic variables and we intend to amend the XLE model to deal with them directly so it can be employed in statistical analysis.

In XLE, the deterministic and statistical delays are given by the following equations:

$$\begin{aligned} D_{primitive} &= F(x, L_{eff}, t_{ox}, V_{th}) && (1) \\ \tilde{D}_{primitive} &= F(x, L_{eff} + \delta_L, t_{ox} + \delta_t, V_{th} + \delta_V) && (2) \end{aligned}$$

F is the delay function, in which δ_L, δ_t and δ_V are statistical variances of the corresponding parameters. x represents the ratio of given primitive gate size to the unit size. Pass-transistors do not have current driving ability, are not widely used in standard logic gates and are not modelled by the XLE method. We model both on and off pass-transistors as an RC network as shown in figure 3 and apply a simple RC analysis. For multiple series-connected pass-transistors, Elmore delay can be utilized to estimate propagation delay. In FPGA interconnect circuits on which we study, pass-transistors are used extensively in multiplexers and tristate-drivers. In view of statistical modelling, resistance is significantly affected by process variation. It is well-known that the equivalent resistance of MOS transistor channel relate with drain-to-source current (I_{ds}) very much. And δ_L, δ_t and δ_V are key parameters of I_{ds} (more precisely the driving ability factor K). So delay formula could be represented as follow similarly. Deterministic and statistical delays are respectively given as equation(3) and equation(4),

$$\begin{aligned} D_{primitive} &= F(x, R, C) && (3) \\ \tilde{D}_{primitive} &= F(x, \tilde{R}, C) && (4) \\ \tilde{R} &= f(x, L_{eff} + \delta_L, t_{ox} + \delta_t, V_{th} + \delta_V) \end{aligned}$$

3. RESEARCH GOAL AND PLAN

Our research goal is to build a model which could be used to analyze and optimize FPGA interconnect delay with consideration of process variation in both deterministic and statistical ways. There are three steps in our plan.

First, we model the interconnect circuits in [1] using the XLE model, and do deterministic delay optimization and sensitivity analysis. Following this work, we will have developed analytic equations to model delay with better accuracy than current RC and LE-based models.

In the second step, we add process variation modelling to the XLE model. Using such a model, optimal transistor sizing in the presence of statistical variation for given interconnect circuits can be determined by optimization. Using Monte Carlo simulation, we will show that such a method considering process variation can lead to better yield than the traditional method of optimizing critical path delay.

In the last stage, benchmark circuits (such as the MCNC benchmarks) will be employed and delay under FPGA interconnect architecture with different deterministic and statistical parameters will be studied. This will be done using the VPR tool, modified with our XLE-based delay model.

4. CONCLUSION

The proposed XLE model will enable us to calculate the delay of FPGA interconnect and determine closed form expressions for optimal transistor size, sensitivity and a minimal bound on delay. We will further extend it to cover process variations, resulting in a tool that can compare the statistical properties of different architectures. The models are simple and relatively technology independent and hence can be used to gain better intuition into the major causes of delay. Such a delay model can be used in optimization models and CAD tools as well as aid designers in developing new FPGA interconnect schemes.

Acknowledgements

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5. REFERENCES

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