



香港中文大學  
計算機科學與工程學系

**CSC 3420**

**Computer Systems Architecture**

**Chapter 5 : The Processor**

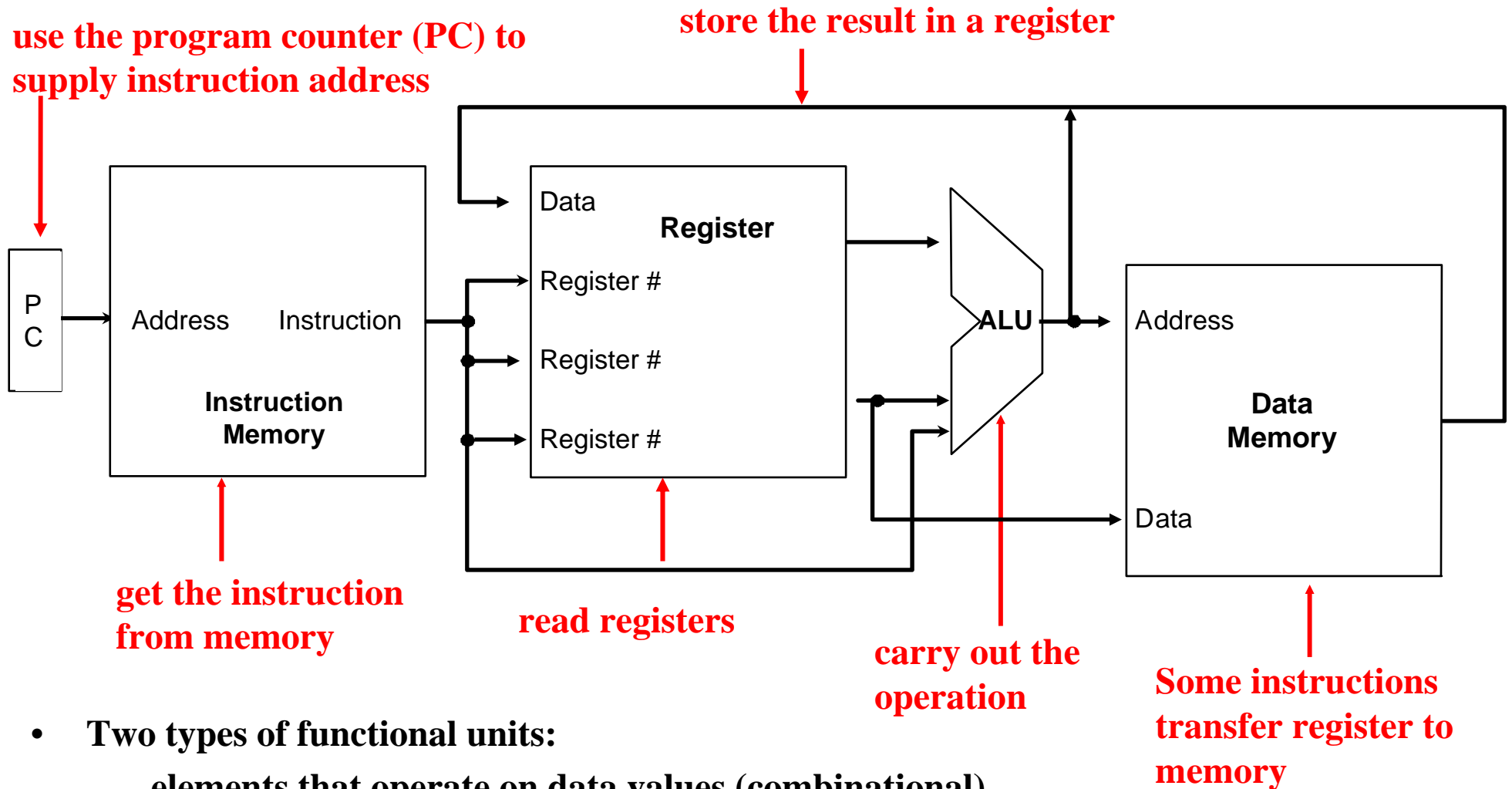
**Data Path and Control**

# The Processor: Datapath & Control

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- We're ready to look at an implementation of a processor (e.g. MIPS)
- **Simplified to contain only:**
  - memory-reference instructions: `lw`, `sw`
  - arithmetic-logical instructions: `add`, `sub`, `and`, `or`, `slt`
  - control flow instructions: `beq`, `j`
- **Generic Implementation:**
  - use the program counter (PC) to supply instruction address
  - get the instruction from memory
  - read registers
  - use the instruction to decide exactly what to do
  - carry out the operation and store the result in a register
- **All instructions use the ALU after reading the registers**
  - ◆ memory-reference
  - ◆ arithmetic
  - ◆ control flow

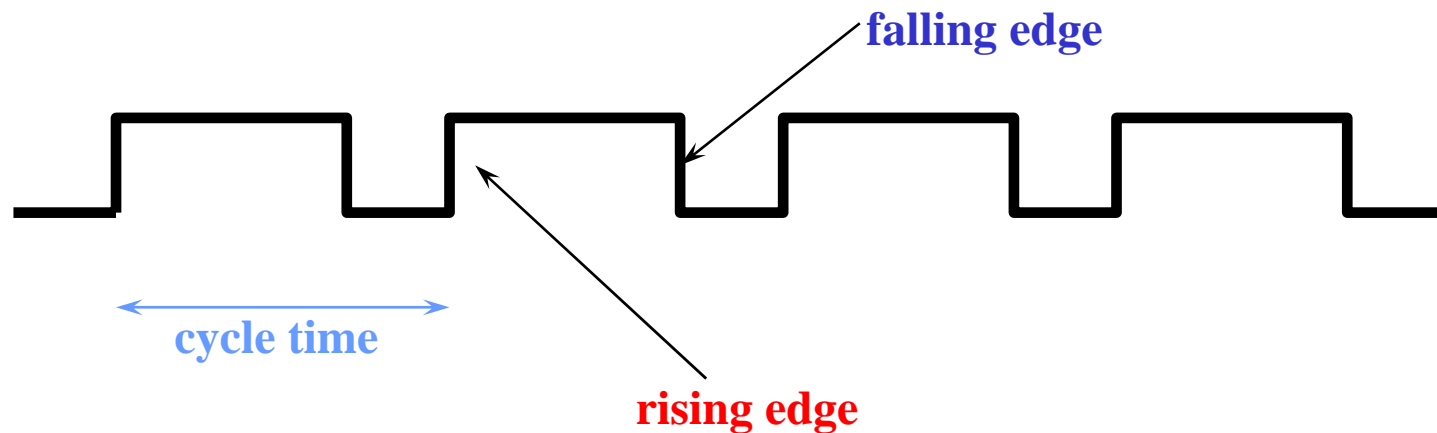
# An Abstract (Simplified) View:



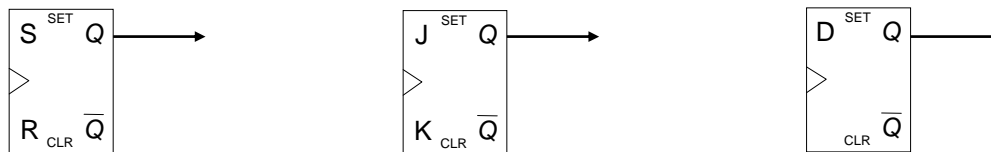
- **Two types of functional units:**
  - elements that operate on data values (combinational)
  - elements that contain states (sequential)

# State Elements

- **Sequential circuits**
- **Can be clocked and not clocked**
- **Clocked circuits (synchronous logic)**
  - **Easier to understand the operations**
  - **Issue is when should an element that contains state be updated**



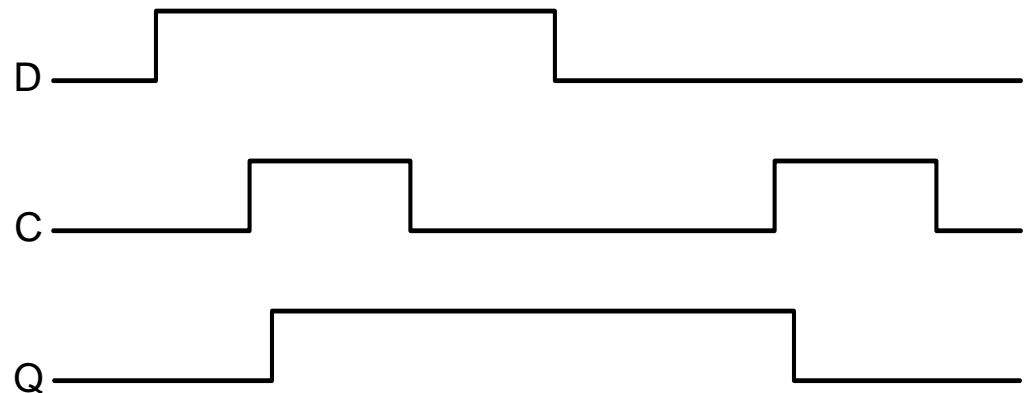
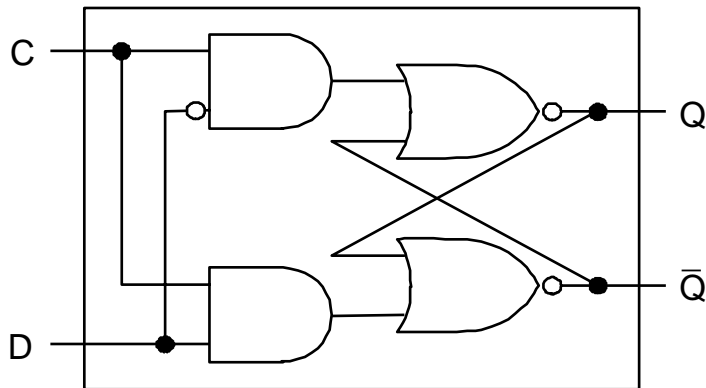
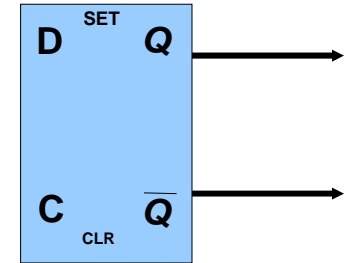
# Latches and Flip-flops



- **Output is always equal to the stored value inside the element**
  - don't need to ask for permission to look at the value
- **Change of state (value) is based on the clock**
- **Clocking methodology**
  - Defines when signals can be read and written
  - Wouldn't want to read a signal at the same time it was being written
- **Latches:**
  - Output responds to input changes only when the clock is asserted
  - Assert means "logically true" (could mean electrically low)
- **Flip-flop:**
  - State changes only on a clock edge
  - (edge-triggered methodology)

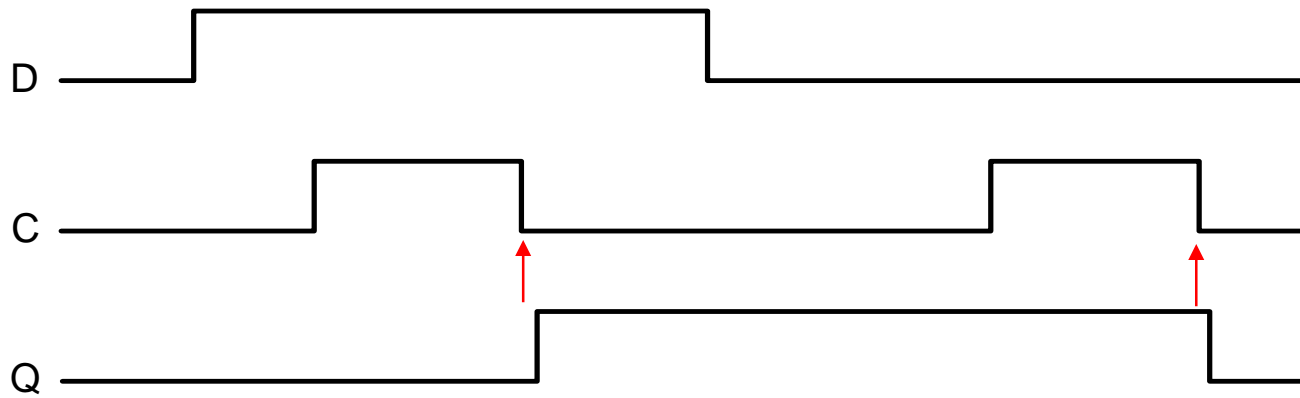
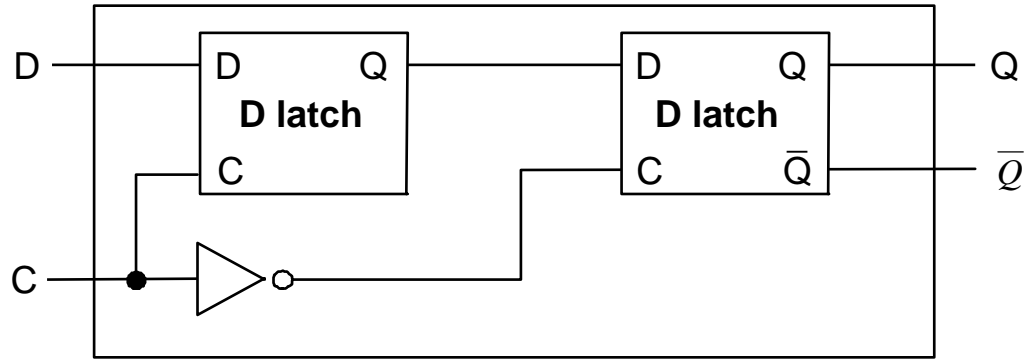
# D-latch

- **Two inputs:**
  - the data value to be stored (**D**)
  - the clock signal (**C**) indicating when to read & store **D**
- **Two outputs:**
  - the value of the internal state (**Q**) and its complement



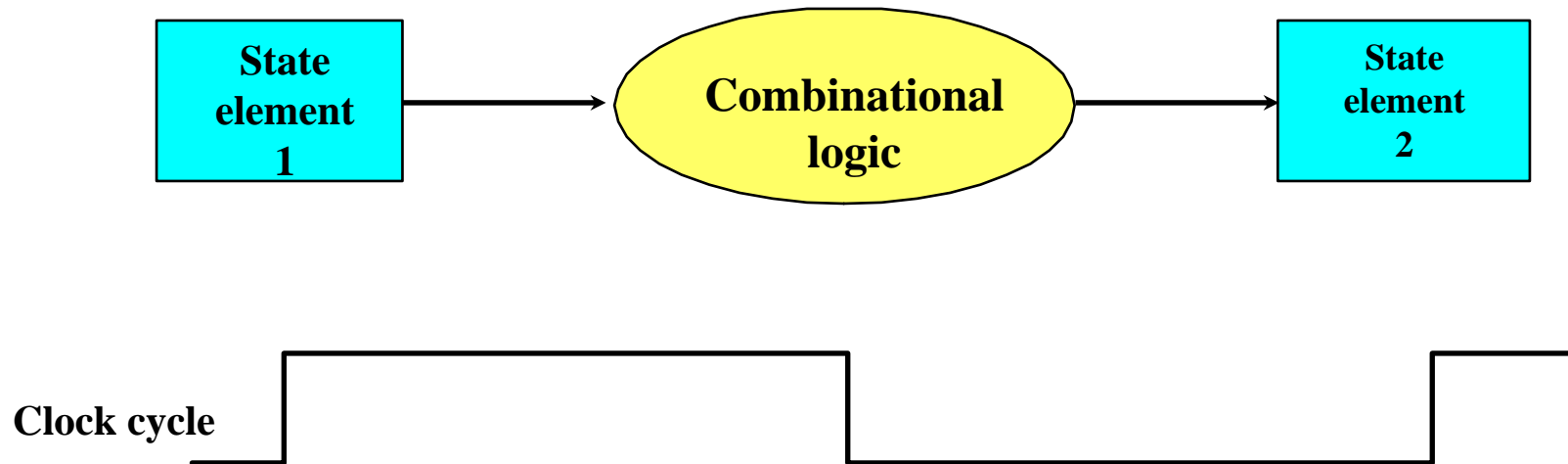
# D flip-flop

- Output changes only on the clock edge



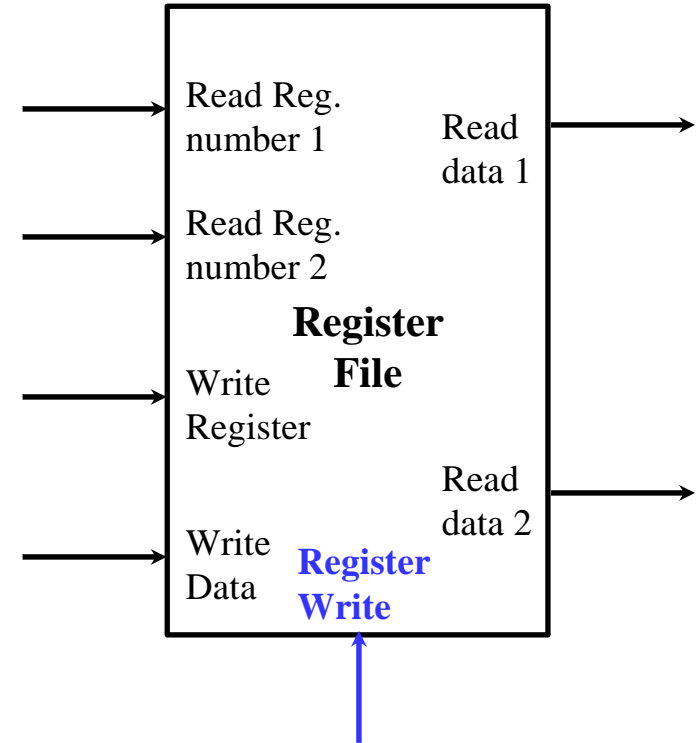
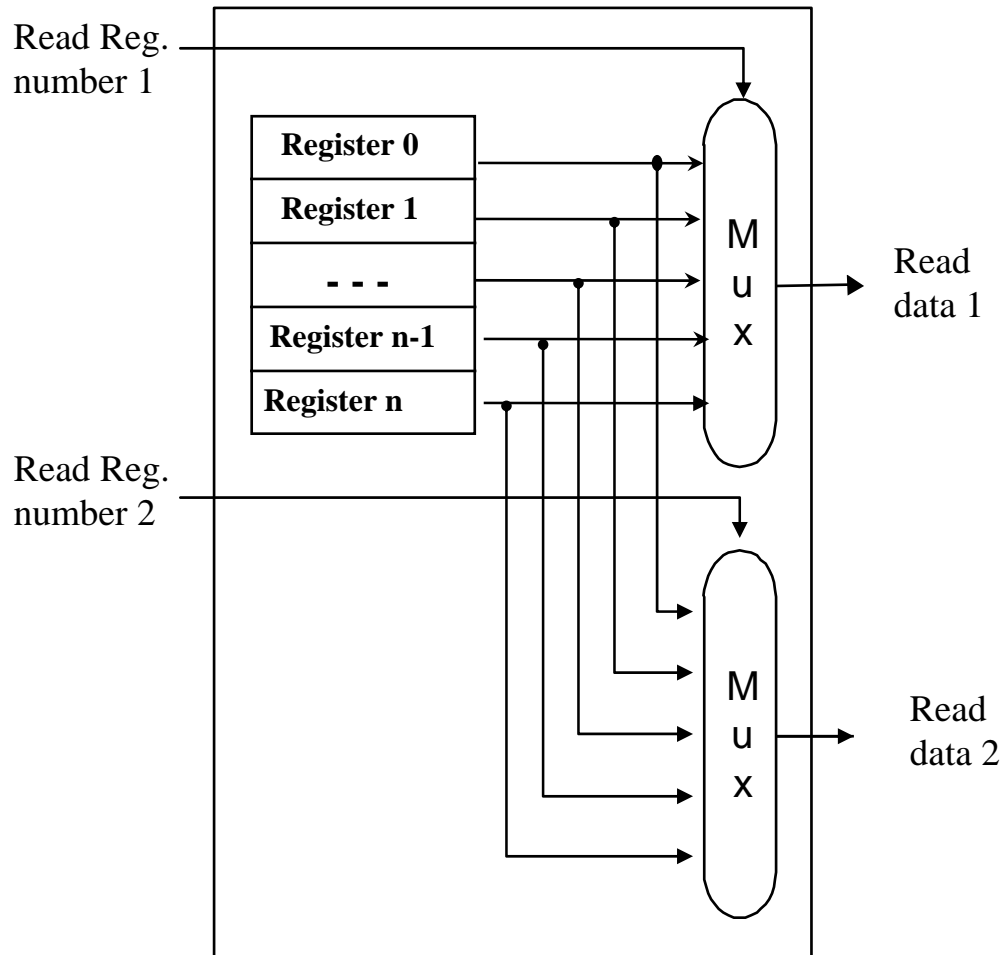
# Our Implementation

- An edge triggered methodology
- Typical execution:
  - read contents of some state elements,
  - send values through some combinational logic
  - write results to one or more state elements



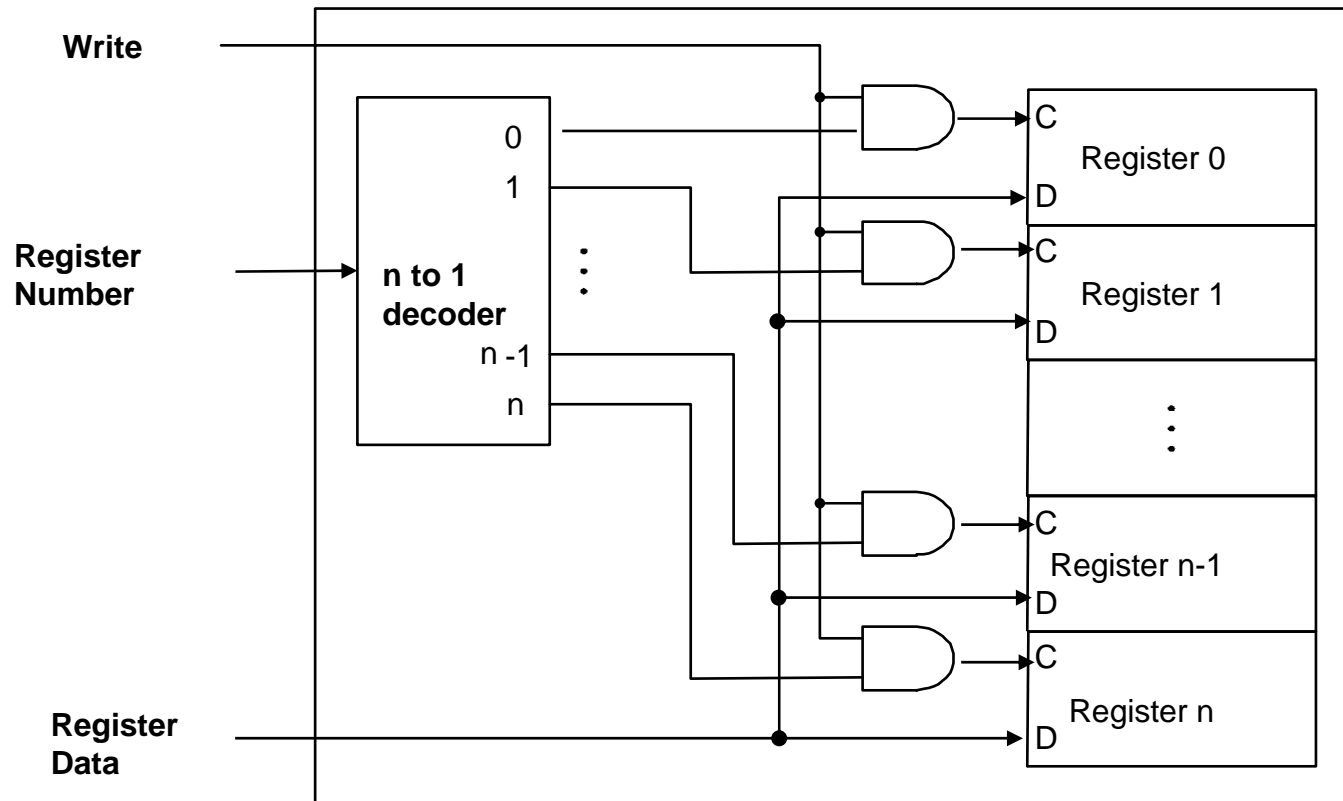
# Register File

- Built using D flip-flops



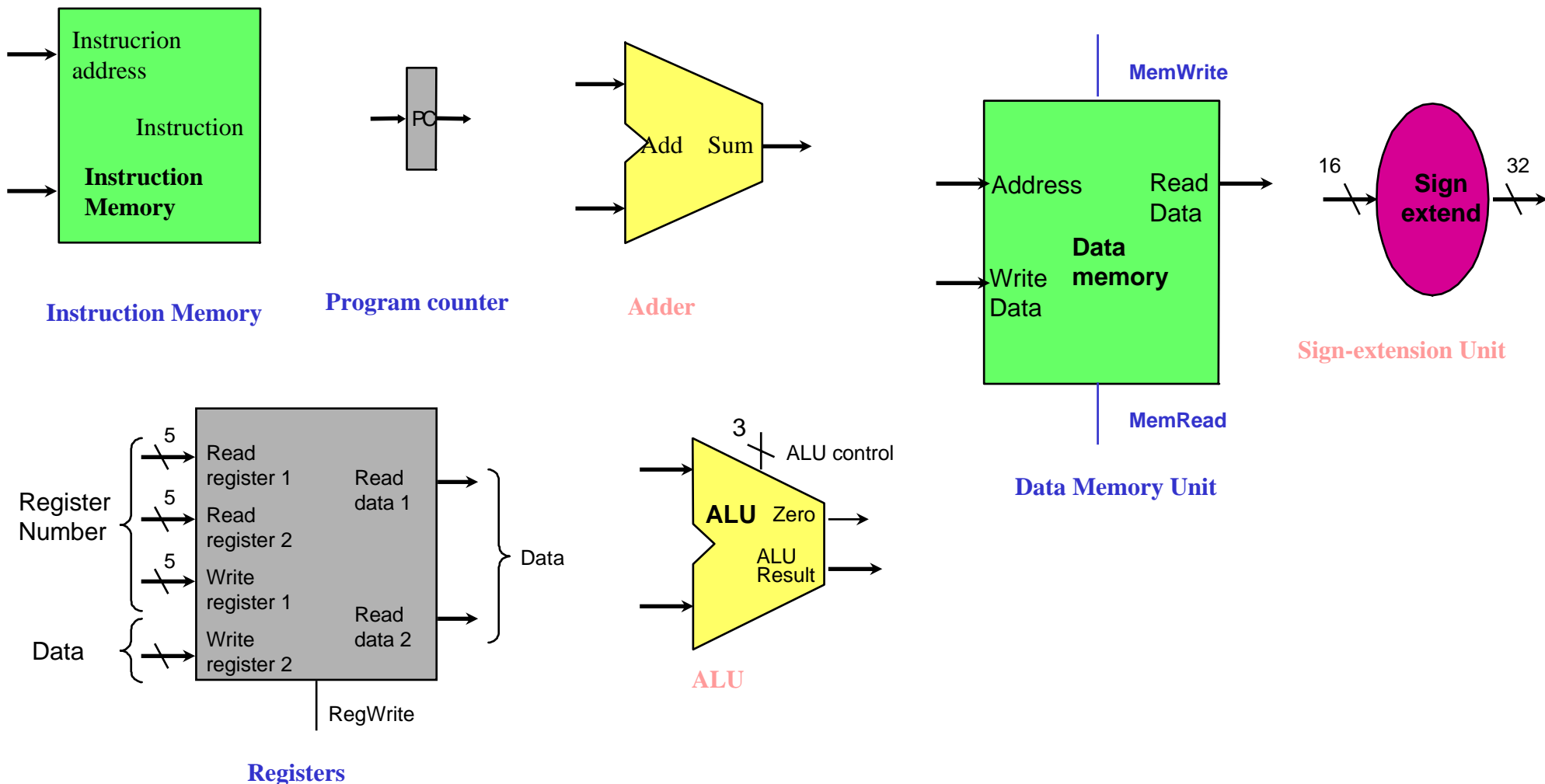
# Register File

- **Note:** we still use the real clock to determine when to write



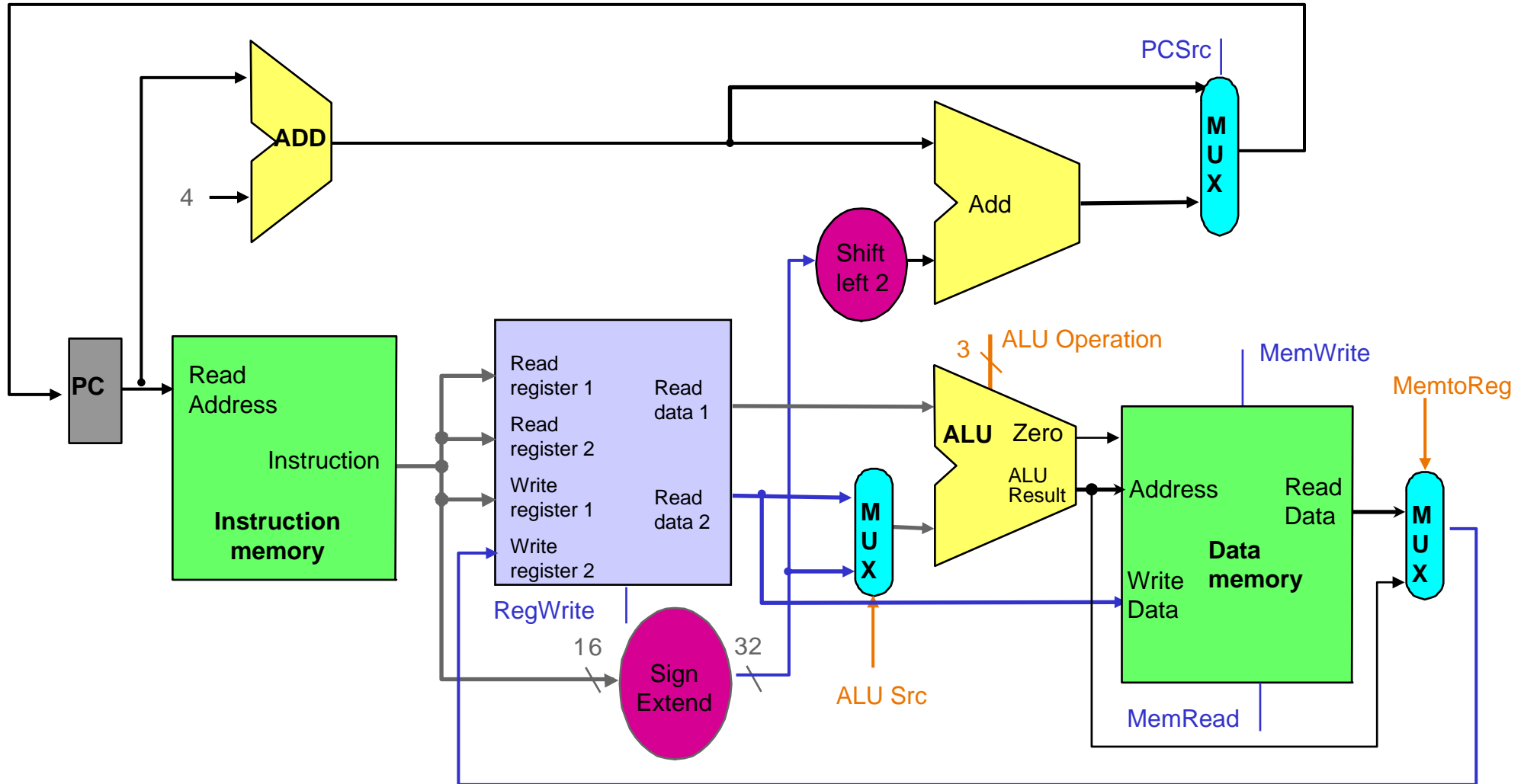
# Simple Implementation

- *What do we need ? Why do we need this stuff?*
- *Include the functional units we need for each instruction*



# Building the Datapath

- Use multiplexers to stitch them together



# Control

- Specify the ALU, and Memory operations
- Control the flow of data by setting multiplexor inputs select controls
- Control Information comes from the 32 bits of the instruction (machine code)
  - ALU's operation based on instruction type and function code
- MIPS Instruction formats :

## a. R-type instruction

<b>0</b>	<b>rs</b>	<b>rt</b>	<b>rd</b>	<b>shamt</b>	<b>funct</b>
<b>31-26</b>	<b>25-21</b>	<b>20-16</b>	<b>15-11</b>	<b>10-6</b>	<b>5-0</b>

## b. Load & Store

<b>35 or 43</b>	<b>rs</b>	<b>rt</b>	<b>address</b>
<b>31-26</b>	<b>25-21</b>	<b>20-16</b>	<b>15 - 0</b>

## c. Branch

<b>4</b>	<b>rs</b>	<b>rt</b>	<b>address</b>
<b>31-26</b>	<b>25-21</b>	<b>20-16</b>	<b>15 - 0</b>

# Control

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- **Example: lw \$1, 100(\$2)**

35	2	1	100
----	---	---	-----

op	rs	rt	16 bit offset
----	----	----	---------------

- **What should the ALU do to complete this instruction?**
- **Need at least 3 bits to describe all ALU functions**

000	AND
001	OR
010	add
110	subtract
111	set-on-less-than

- **Why is the code for subtract 110 and not 011?**

# Control: ALU control signals

- Classify instruction types and encode it into a 2-bit code
  - 00 = lw, sw                      **Memory Transfer**
  - 01 = beq,                        **Flow control**
  - 10 = arithmetic                **R-type**
- For Arithmetic type, the exact function is specified in the function field
- Must translate the 2-bit instruction type and the 6-bit functions code into a 3-bit ALU control signals
  - Translation can be specified by a truth table which can later turn into gates

Instruction Opcode	ALUOp	Instruction Operation	Function field	Desired ALU action	ALU control input
			F5 F4 F3 F2 F1 F0		
LW	00	load word	X X X X X X	add	0 1 0
SW	00	store word	X X X X X X	add	0 1 0
Branch equal	01	branch equal	X X X X X X	subtract	1 1 0
R-type	10	add	1 0 0 0 0 0	add	0 1 0
R-type	10	subtract	1 0 0 0 1 0	subtract	1 1 0
R-type	10	AND	1 0 0 1 0 0	and	0 0 0
R-type	10	OR	1 0 0 1 0 1	or	0 0 1
R-type	10	set on less than	1 0 1 0 1 0	set on less than	1 1 1

# Control: Translating specs into logic gates

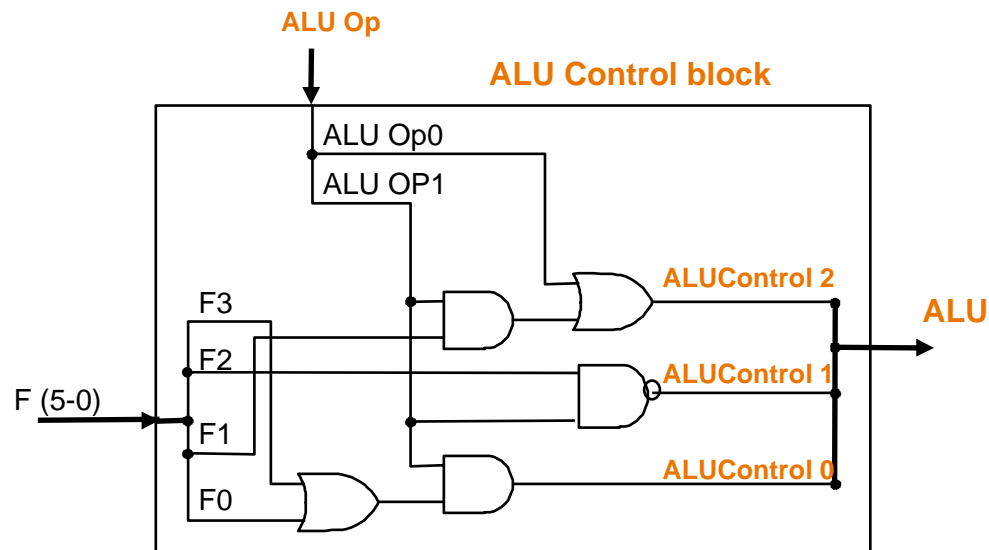
Instruction Opcode	ALUOp [1, 0]	Instruction Operation	Function field						Desired ALU action	ALU control [2, 1, 0]		
			F5	F4	F3	F2	F1	F0				
LW	0 0	load word	X	X	X	X	X	X	add	0	1	0
SW	0 0	store word	X	X	X	X	X	X	add	0	1	0
Branch equal	0 1	branch equal	X	X	X	X	X	X	subtract	1	1	0
R-type	1 0	add	1	0	0	0	0	0	add	0	1	0
R-type	1 0	subtract	1	0	0	0	1	0	subtract	1	1	0
R-type	1 0	AND	1	0	0	1	0	0	and	0	0	0
R-type	1 0	OR	1	0	0	1	0	1	or	0	0	1
R-type	1 0	set on less than	1	0	1	0	1	0	set on less than	1	1	1

- Simple combinational logic
- Apply the tricks you have learnt in Digital Logic

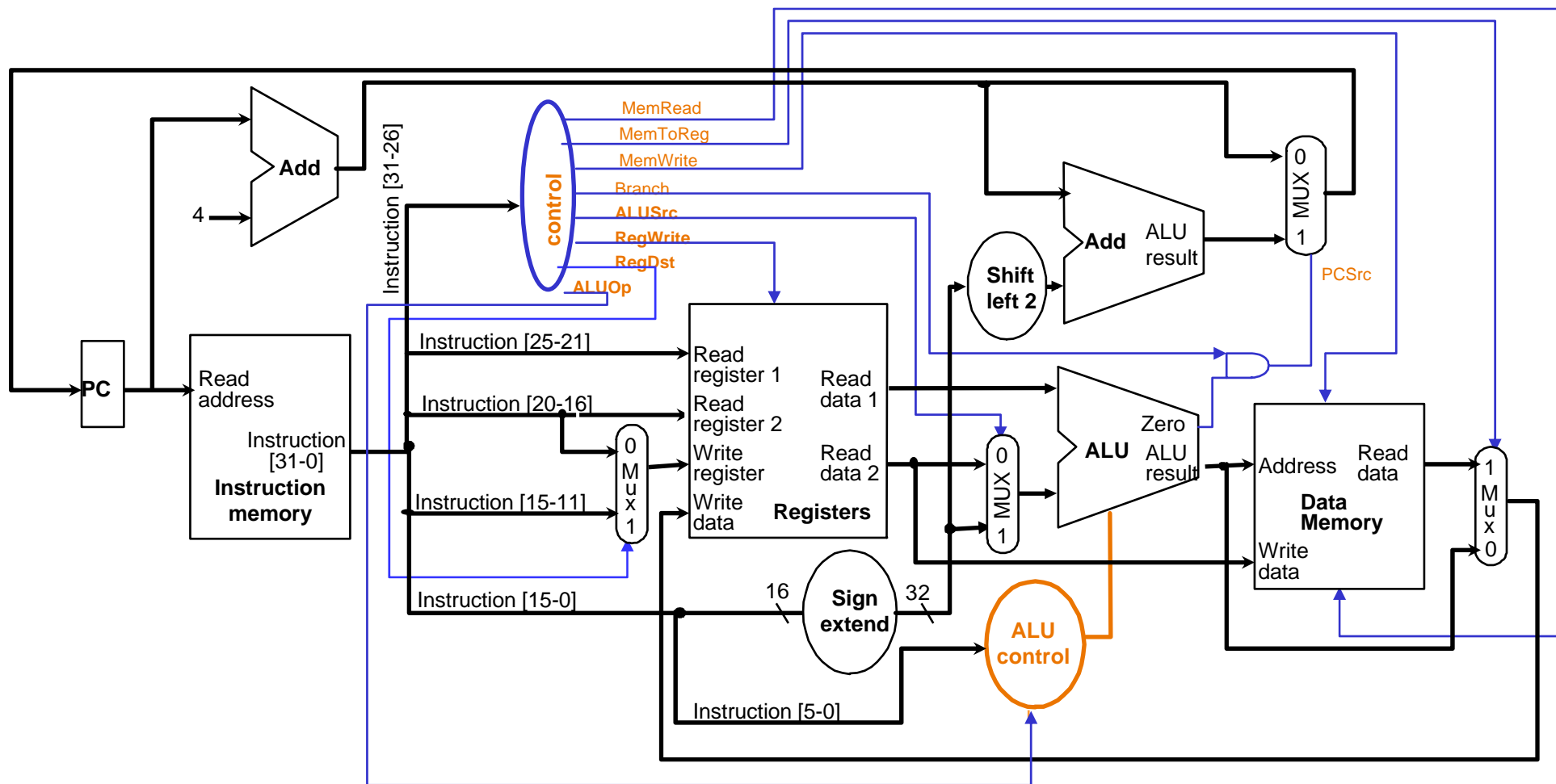
$$ALUControl_0 = ALUOP_1 \cdot (F_0 + F_3)$$

$$ALUControl_1 = \overline{ALUOP_1} \cdot F_2$$

$$ALUControl_2 = ALUOP_1 \cdot F_1 + ALUOP_0$$



# Control: Multiplexer control signals

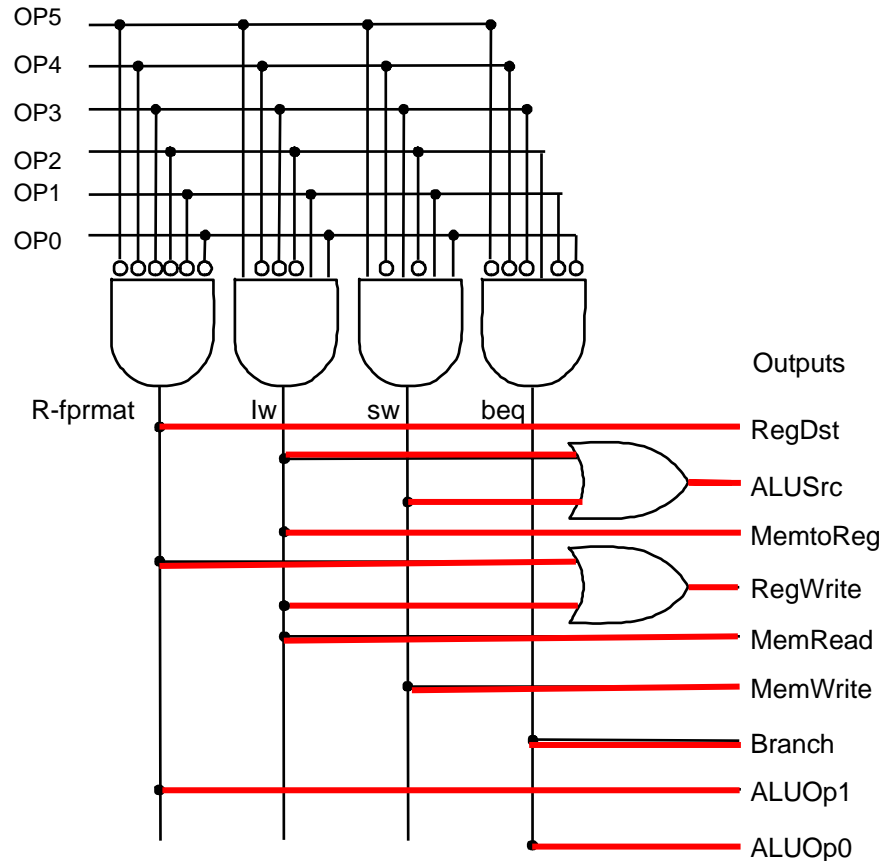


Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUOp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

# Control: Generate the multiplexer control signals

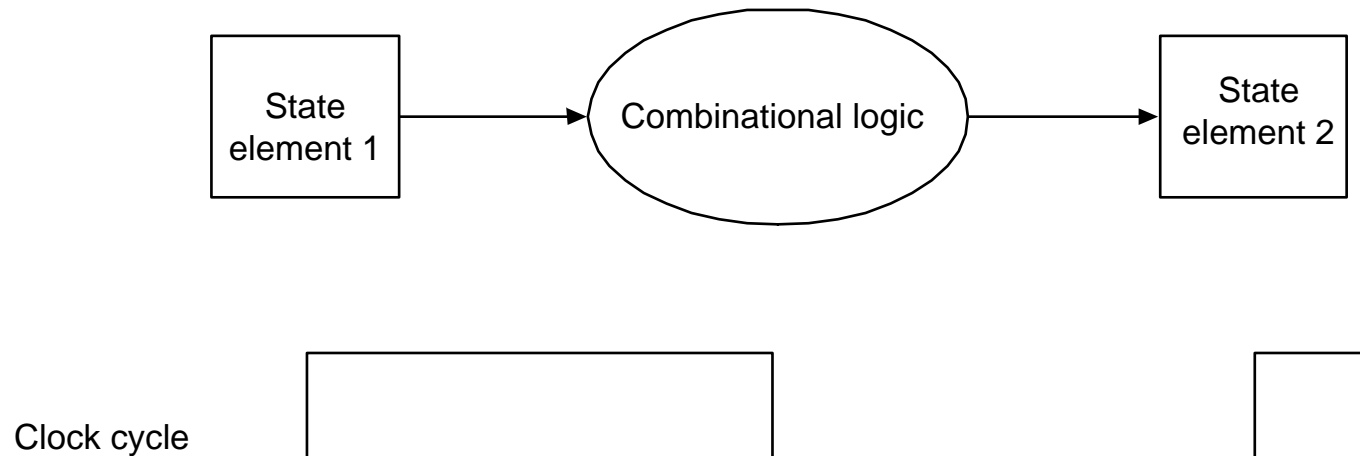
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

Inputs



# Our Simple Control Structure

- Control logics and ALU are combinational logic circuits
- We wait for everything to settle down, and the right thing to be done
  - ALU might not produce “correct answer” right away
  - we use write signals along with clock to determine when to write
- **Cycle time** determined by length of the **longest path**

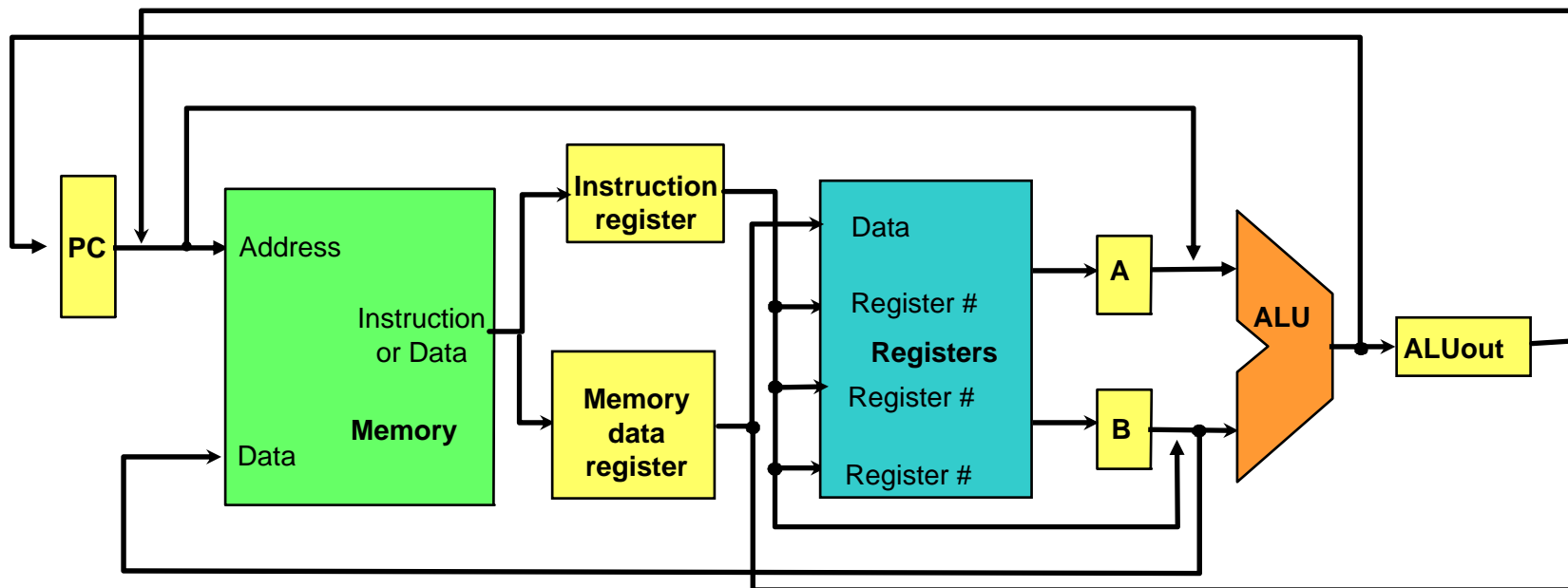


*To understand the operations, we are ignoring some details like setup and hold times*



# Where we are the pitfalls

- **Single Cycle Problems:**
  - what if we had a more complicated instruction like floating point?
  - **Wasteful:** short cycle for simple instructions will become longer
- **One Solution:**
  - use a “smaller” cycle time
  - have different instructions taking different numbers of cycles
  - a “**multicycle**” datapath:



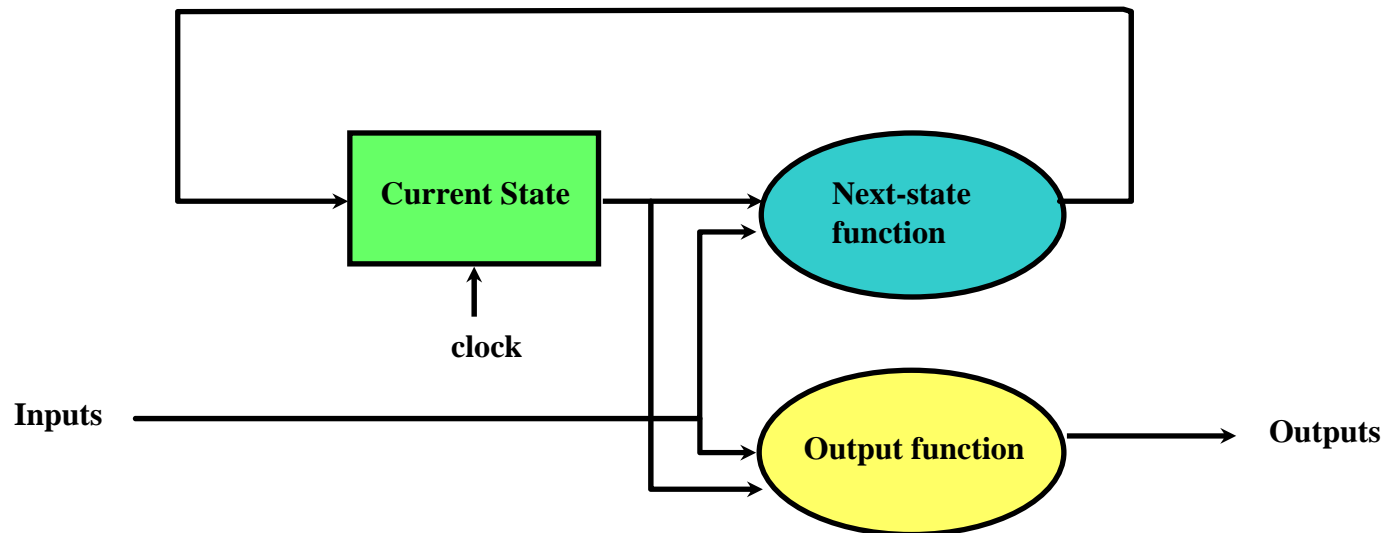
# Multi-cycle Approach

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- We will be **reusing functional units**
  - ALU used to compute address and to increment PC
  - Memory used for instruction and data
- Our control signals will not be determined solely by instruction
  - e.g., what should the ALU do for a “subtract” instruction?
  - It is also a function of the states
- We’ll use a finite state machine for control to specify the action steps

# Review: finite state machines

- **Finite state machines:**
  - a set of states and
  - next state function (determined by current state and the input)
  - output function (determined by current state and **possibly input**)



- We'll use a **Moore machine** (outputs based only on current state only)

# Review: finite state machines

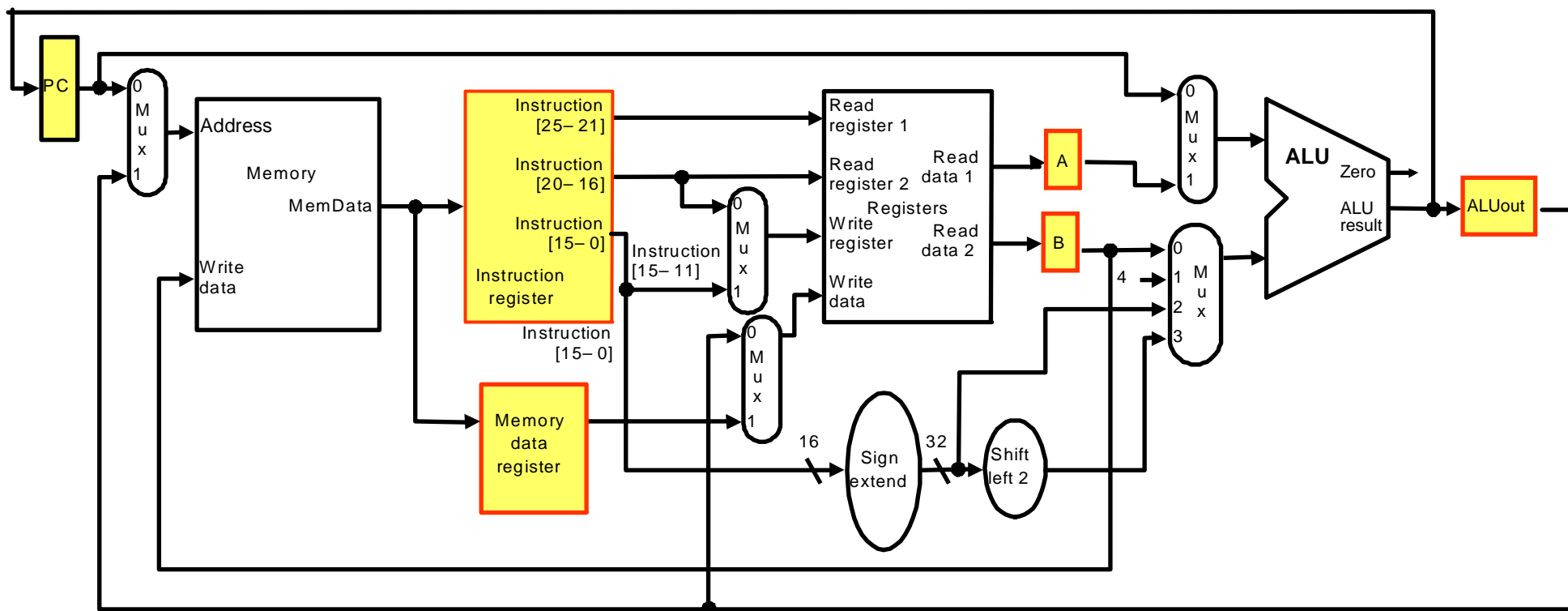
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- **Example:**

**B. 21** *A friend would like you to build an “electronic eye” for use as a fake security device. The device consists of three lights lined up in a row, controlled by the outputs Left, Middle, and Right, which, if asserted, indicate that a light should be on. Only one light is on at a time, and the light “moves” from left to right and then from right to left, thus scaring away thieves who believe that the device is monitoring their activity. Draw the graphical representation for the finite state machine used to specify the electronic eye. Note that the rate of the eye’s movement will be controlled by the clock speed (which should not be too great) and that there are essentially no inputs.*

# Multi-cycle Approach

- Break up the instructions into steps, each step takes a cycle
  - balance the amount of work to be done
  - restrict each cycle to use only one major functional unit
- At the end of a cycle
  - store values for use in later cycles (easiest thing to do)
  - introduce additional “internal” registers



# Five Execution Steps

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- **Instruction Fetch**
- **Instruction Decode and Register Fetch**
- **Execution, Memory Address Computation, or Branch Completion**
- **Memory Access or R-type instruction completion**
- **Write-back step**

***INSTRUCTIONS TAKE FROM 3 - 5 CYCLES!***

# Step 1: Instruction Fetch

---

- Use PC to get instruction and put it in the Instruction Register.
- Increment the PC by 4 and put the result back in the PC.
- Can be described succinctly using RTL "Register-Transfer Language"

```
IR = Memory[PC];  
PC = PC + 4;
```

*Can we figure out the values of the control signals?*

*What is the advantage of updating the PC now?*

## Step 2: Instruction Decode and Register Fetch

---

- **Read registers  $rs$  and  $rt$  in case we need them**
- **Compute the branch address in case the instruction is a branch**

- **RTL:**

```
A = Reg[IR[25-21]];
```

```
B = Reg[IR[20-16]];
```

```
ALUOut = PC + (sign-extend(IR[15-0]) << 2);
```

- **We aren't setting any control lines based on the instruction type (we are busy "decoding" it in our control logic)**

## Step 3 (instruction dependent)

---

- **ALU is performing one of three functions, based on instruction type**

- **Memory Reference:**

```
ALUOut = A + sign-extend(IR[15-0]);
```

- **R-type:**

```
ALUOut = A op B;
```

- **Branch:**

```
if (A==B) PC = ALUOut;
```

## Step 4 (R-type or memory-access)

---

- Loads and stores access memory

```
MDR = Memory[ALUOut];
```

or

```
Memory[ALUOut] = B;
```

- R-type instructions finish

```
Reg[IR[15-11]] = ALUOut;
```

- *The write actually takes place at the end of the cycle on the edge*

# Write-back step

- $\text{Reg}[\text{IR}[20-16]] = \text{MDR};$

*What about all the other instructions?*

## Summary

Step name	Action for R-type instructions	Action for memory-reference instructions	Action for branches	Action for jumps
Instruction fetch	$\text{IR} = \text{Memory}[\text{PC}]$ $\text{PC} = \text{PC} + 4$			
Instruction decode/register fetch	$A = \text{Reg}[\text{IR}[25-21]]$ $B = \text{Reg}[\text{IR}[20-16]]$ $\text{ALUOut} = \text{PC} + (\text{sign-extend}(\text{IR}[15-0]) \ll 2)$			
Execution, address computation, branch/jump completion	$\text{ALUOut} = A \text{ op } B$	$\text{ALUOut} = A + \text{sign-extend}(\text{IR}[15-0])$	if $(A == B)$ then $\text{PC} = \text{ALUOut}$	$\text{PC} = \text{PC}[\text{31-28}] \parallel (\text{IR}[25-0] \ll 2)$
Memory access or R-type completion	$\text{Reg}[\text{IR}[15-11]] = \text{ALUOut}$	Load: $\text{MDR} = \text{Memory}[\text{ALUOut}]$ or Store: $\text{Memory}[\text{ALUOut}] = B$		
Memory read completion		Load: $\text{Reg}[\text{IR}[20-16]] = \text{MDR}$		

# Check your understanding

---

- How many cycles will it take to execute this code?

```
lw $t2, 0($t3)
lw $t3, 4($t3)
beq $t2, $t3, Label          #assume not taken
add $t5, $t2, $t3
sw $t5, 8($t3)
```

Label: ...

- What is going on during the 8th cycle of execution?
- In what cycle does the actual addition of \$t2 and \$t3 takes place?

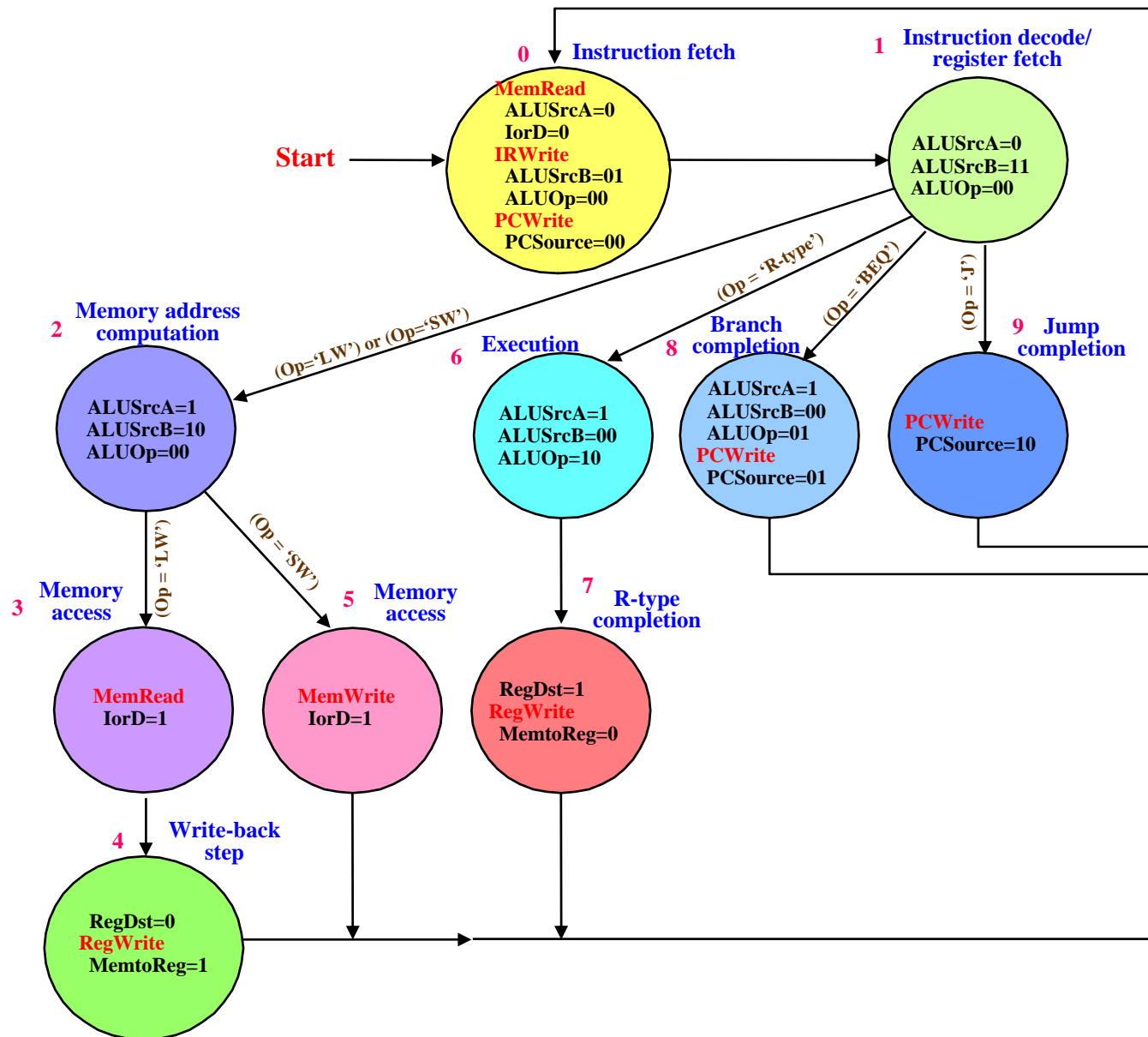


# Implementing the Control

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- **Value of control signals is dependent upon:**
  - **what instruction is being executed**
  - **which step is being performed**
- **Use the information we've accumulated to specify a finite state machine**
  - **specify the finite state machine graphically, or**
  - **use microprogramming**
- **Implementation can be derived from specification**

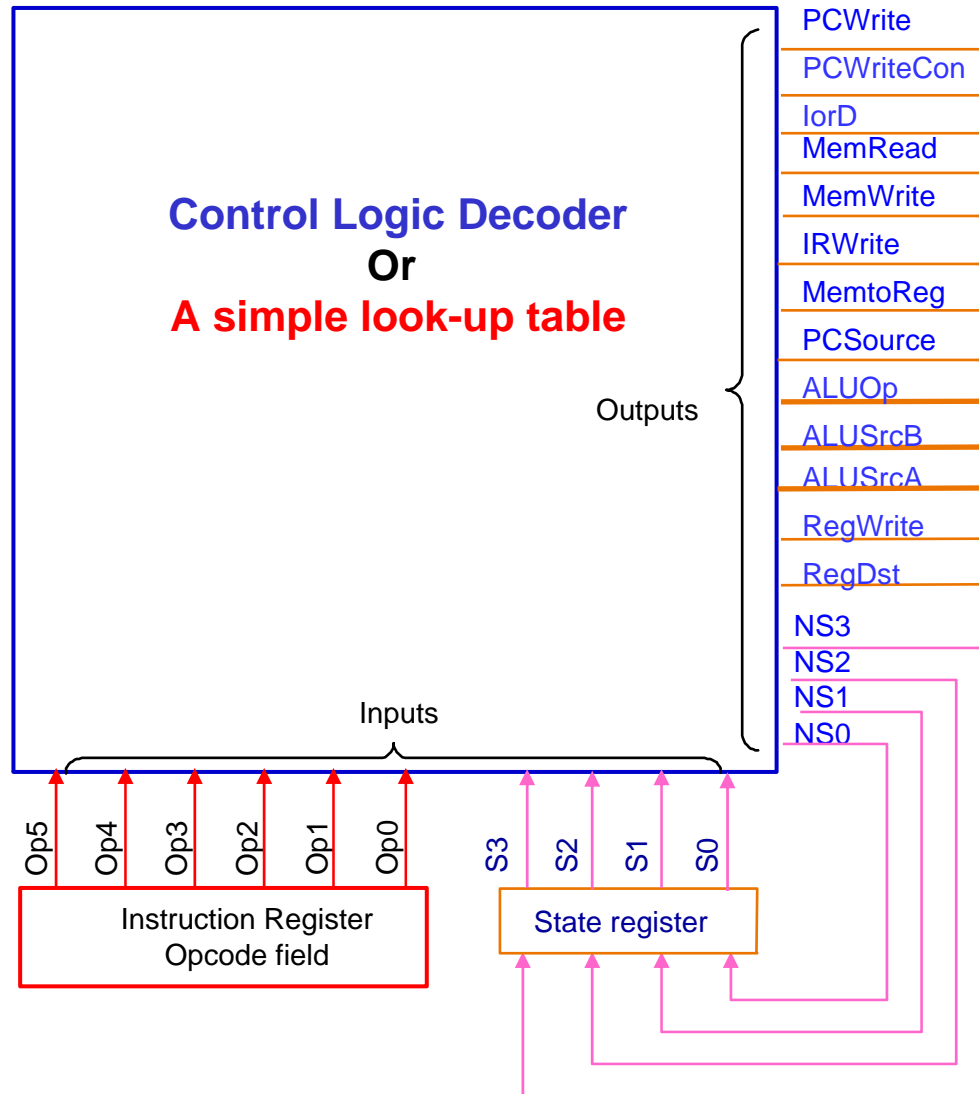
# Graphical Specification of FSM



How many state bits will we need?

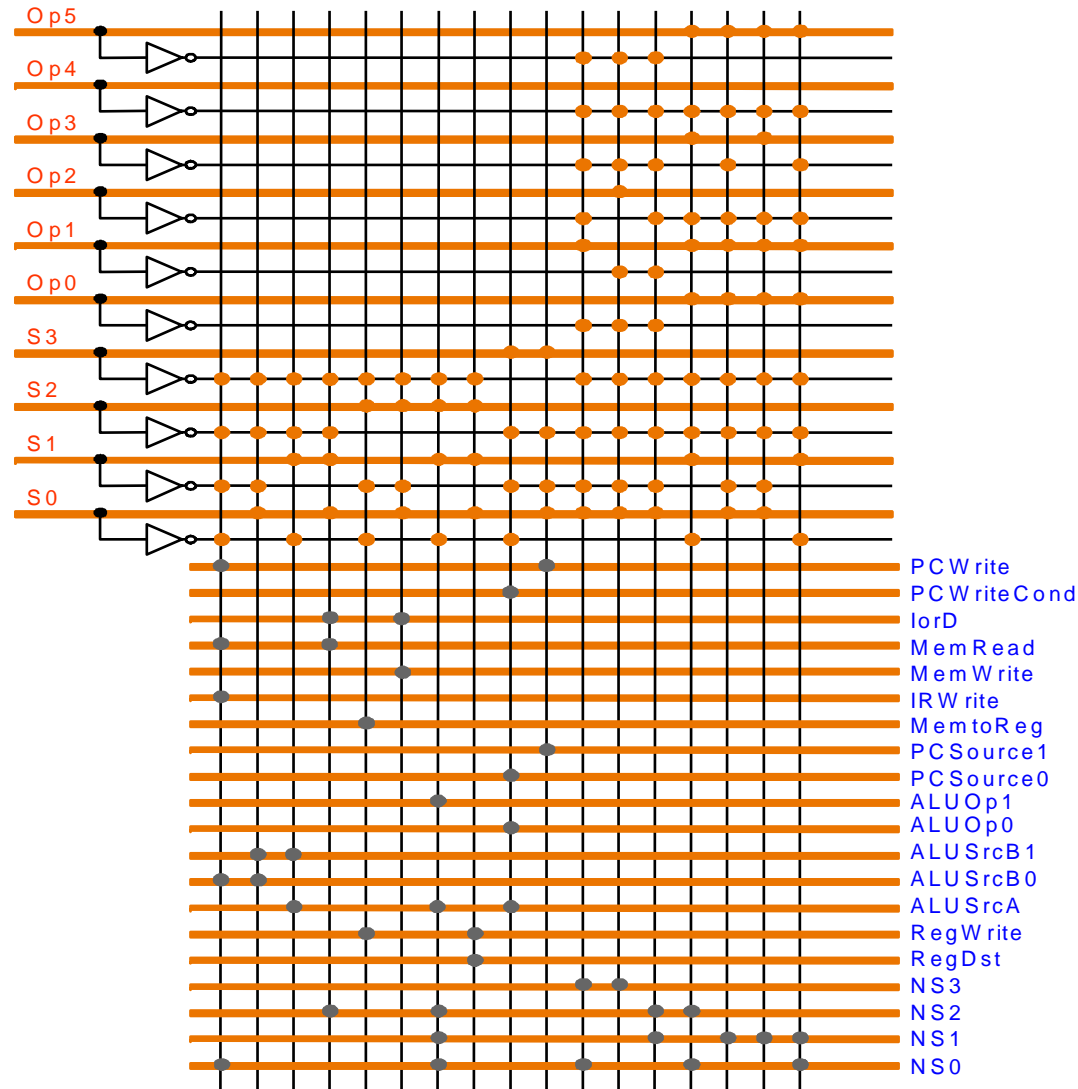
# Finite State Machine for Control

- Implementation:



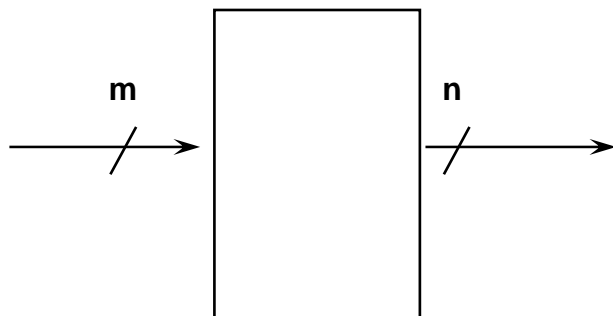
# PLA Implementation

- If I picked a horizontal or vertical line could you explain it?



# ROM Implementation

- **ROM = "Read Only Memory"**
  - values of memory locations are fixed ahead of time
- **A ROM can be used to implement a truth table**
  - if the address is  $m$ -bits, we can address  $2^m$  entries in the ROM.
  - our outputs are the bits of data that the address points to.

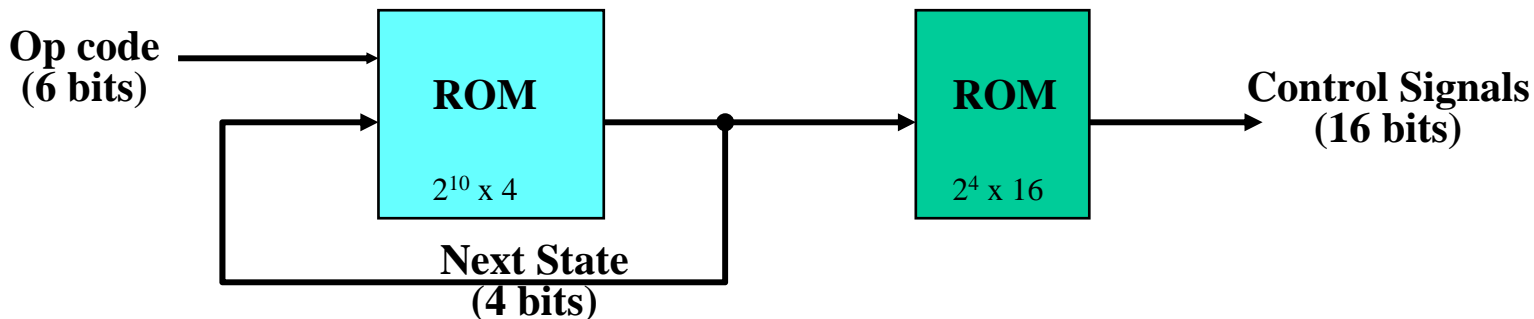


0	0	0	0	0	1	1
0	0	1	1	1	0	0
0	1	0	1	1	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1

**$m$  is the "height", and  $n$  is the "width"**

# ROM Implementation

- **How many inputs are there?**  
6 bits for opcode, 4 bits for state = 10 address lines  
(i.e.,  $2^{10} = 1024$  different addresses)
- **How many outputs are there?**  
16 datapath-control outputs, 4 state bits = 20 outputs
- **ROM is  $2^{10} \times 20 = 20\text{K}$  bits (and a rather unusual size)**
  - Rather wasteful, since for lots of the entries, the outputs are the same
    - i.e., opcode is often ignored
- **How to minimize the ROM size?**
  - Break up the table into two parts
    - 4 state bits tell you the 16 outputs,  $2^4 \times 16$  bits of ROM
    - 10 bits tell you the 4 next state bits,  $2^{10} \times 4$  bits of ROM
    - Total: 4.3K bits of ROM



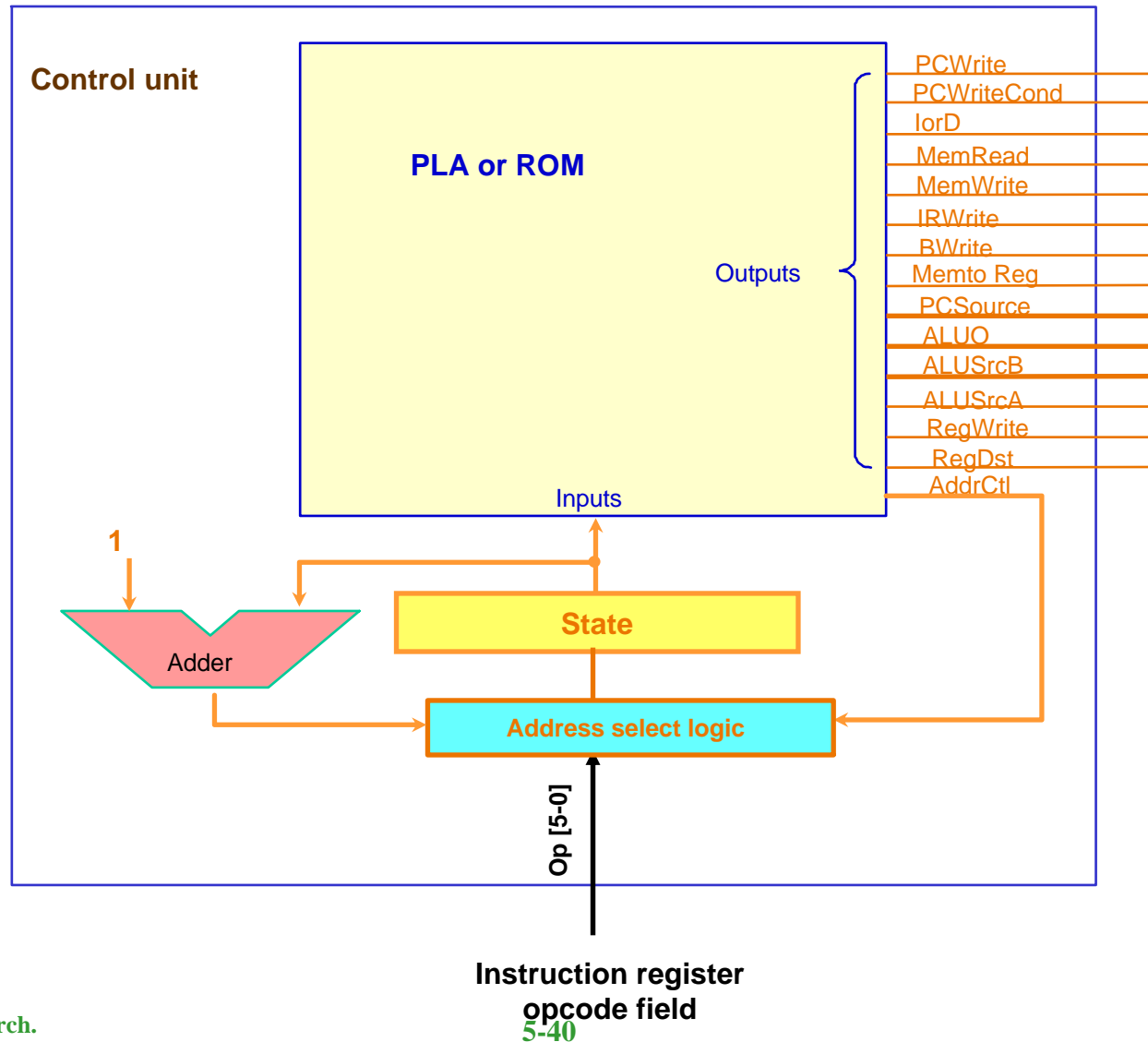
# ROM versus PLA

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- **PLA is much smaller**
  - can share product terms
  - only need entries that produce an active output
  - can take into account don't cares
- **Size is (#inputs \* #product-terms) + (# product-terms \* #outputs)**  
For this example =  $(10 \times 17) + (17 \times 20) = 460$  PLA cells
- **PLA cells usually about the size of a ROM cell (slightly bigger)**

# Another Implementation Style

- Complex instructions: the "next state" is often current state + 1

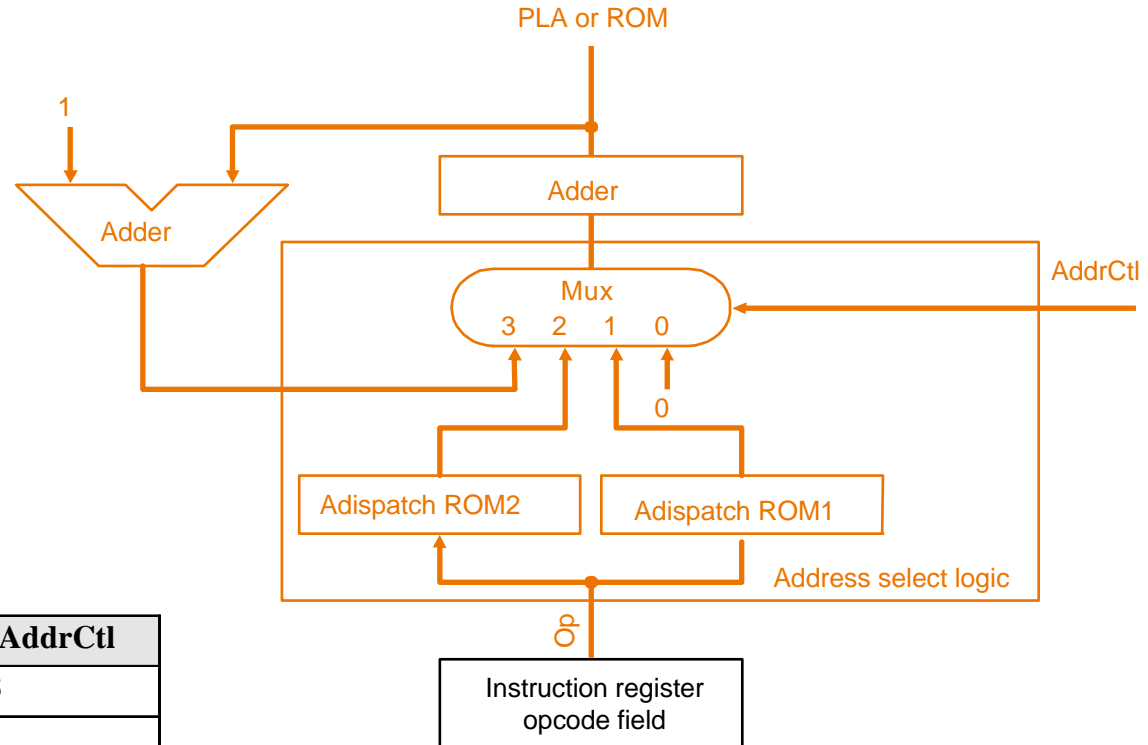


# Details

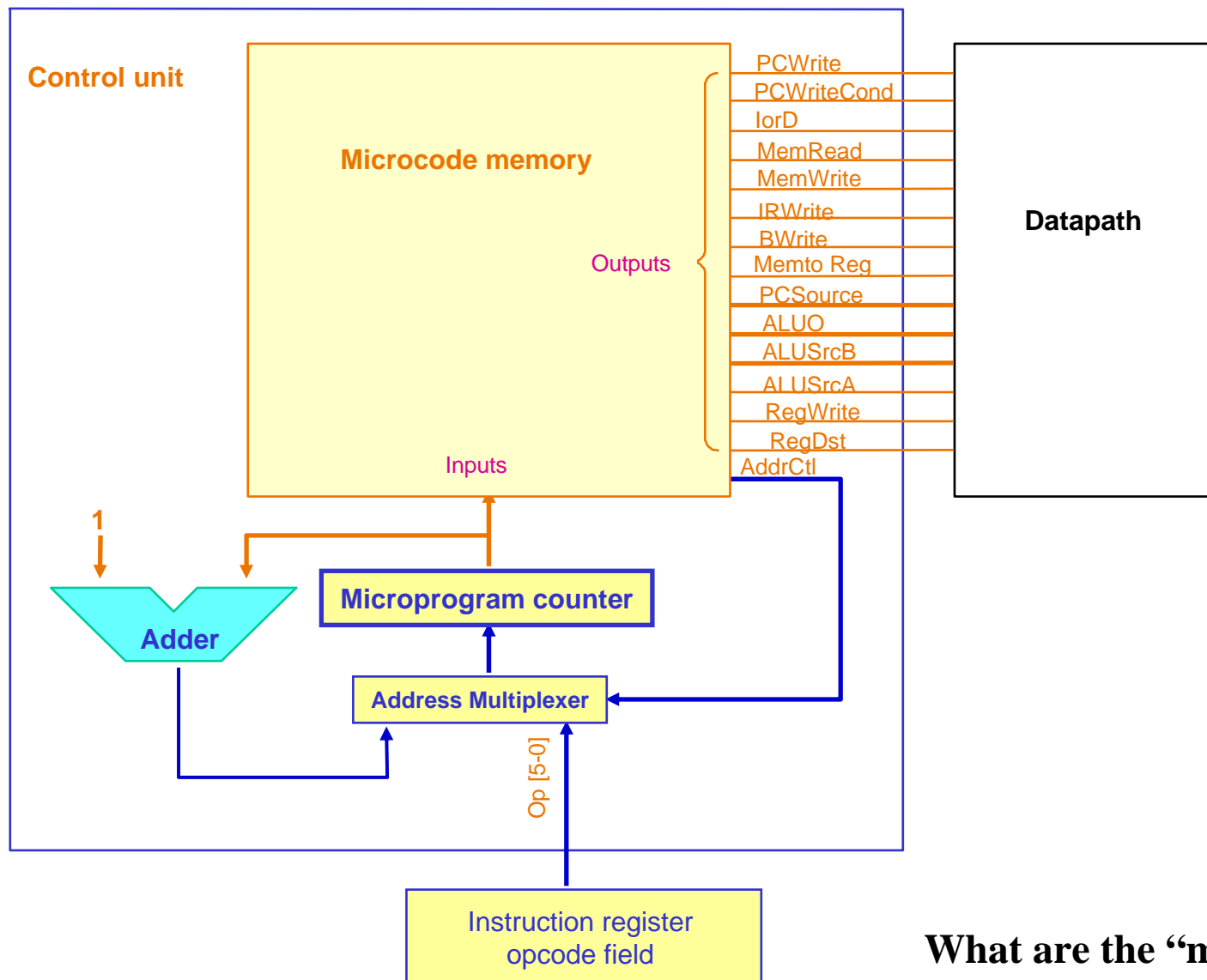
Dispatch ROM1		
OP	Opcode name	Value
000000	R-format	0110
000010	jmp	1001
000100	beq	1000
100011	lw	0010
101011	sw	0010

Dispatch ROM2		
Op	Opcode name	Value
100011	lw	0011
101011	sw	0101

State number	Address-control action	Value of AddrCtl
0	Use incremented state	3
1	Use dispatch ROM1	1
2	Use dispatch ROM2	2
3	Use incremented state	3
4	Replace state number 0	0
5	Replace state number 0	0
6	Use incremented state	3
7	Replace state number 0	0
8	Replace state number 0	0
9	Replace state number 0	0



# Microprogramming



What are the “microinstructions” ?

# Microprogramming

- **A specification methodology**
  - appropriate if hundreds of opcodes, modes, cycles, etc.
  - signals specified symbolically using microinstructions

Label	ALU control	SRC1	SRC2	Register control	Memory	PCWrite control	Sequencing
Fetch	Add	PC	4		Read PC	ALU	Seq
	Add	PC	Extshft	Read			Dispatch 1
Mem1	Add	A	Extend				Dispatch 2
LW2					Read ALU		Seq
				Write MDR			Fetch
SW2					Write ALU		Fetch
Rformat1	Func code	A	B				Seq
				Write ALU			Fetch
BEQ1	Subt	A	B			ALUOut-cond	Fetch
JUMP1						Jump address	Fetch

- *Will two implementations of the same architecture have the same microcode?*
- *What would a microassembler do?*

# Microinstruction format

Field name	Value	Signals active	Comment
ALU control	Add	ALUOp = 00	Cause the ALU to add.
	Subt	ALUOp = 01	Cause the ALU to subtract; this implements the compare for branches
	Func code	ALUOp = 10	Use the instruction's function code to determine ALU control.
SRC1	PC	ALUSrcA = 0	Use the PC as the first ALU input.
	A	ALUSrcA = 1	Register A is the first ALU input.
SRC2	B	ALUSrcB = 00	Register B is the second ALU input.
	4	ALUSrcB = 01	Use 4 as the second ALU input.
	Extend	ALUSrcB = 10	Use output of the sign extension unit as the second ALU input.
	Extshft	ALUSrcB = 11	Use the output of the shift-by-two unit as the second ALU input.
Register control	Read		Read two registers using the rs and rt fields of the IR as the register numbers and putting the data into registers A and B.
	Write ALU	RegWrite, RegDst = 1, MemtoReg = 0	Write a register using the rd field of the IR as the register number and the contents of the ALUOut as the data.
	Write MDR	RegWrite, RegDst = 0, MemtoReg = 1	Write a register using the rt field of the IR as the register number and the contents of the MDR as the data.
Memory	Read PC	MemRead, lorD = 0	Read memory using the PC as address; write result into IR (and the MDR).
	Read ALU	MemRead, lorD = 1	Read memory using the ALUOut as address; write result into MDR.
	Write ALU	MemWrite, lorD = 1	Write memory using the ALUOut as address, contents of B as the data.
PC write control	ALU	PCSource = 00 PCWrite	Write the output of the ALU into the PC.
	ALUOut-cond	PCSource = 01, PCWriteCond	If the Zero output of the ALU is active, write the PC with the contents of the register ALUOut.
	jump address	PCSource = 10, PCWrite	Write the PC with the jump address from the instruction.
Sequencing	Seq	AddrCtl = 11	Choose the next microinstruction sequentially.
	Fetch	AddrCtl = 00	Go to the first microinstruction to begin a new instruction.
	Dispatch 1	AddrCtl = 01	Dispatch using the ROM 1.
	Dispatch 2	AddrCtl = 10	Dispatch using the ROM 2.

# Maximally versus Minimally Encoded

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- **No encoding:**
  - 1 bit for each datapath operation
  - faster, requires more memory (logic)
  - used for VAX 780 — an astonishing 400K of memory!
- **Lots of encoding:**
  - send the microinstructions through logic to generate control signals
  - uses less memory, slower
- **Historical context of CISC:**
  - Too much logic to put on a single chip with everything else
  - Use a ROM (or even RAM) to hold the microcode
  - It's easy to add new instructions

# Microcode: Trade-offs

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- **Distinction between specification and implementation is sometimes blurred**
- **Specification Advantages:**
  - Easy to design and write
  - Design architecture and microcode in parallel
  - Needs supporting tools
- **Implementation (off-chip ROM) Advantages**
  - Easy to change since values are in memory
  - Can emulate other architectures
  - Can make use of internal registers
- **Technology has changed: RAM is preferred**
  - Control is implemented on same chip as processor
  - ROM is no longer faster than RAM
  - No need to go back and make changes

# The Big Picture

